Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Input 1**
2. **Drain 1**
3. **Source 1**
4. **V-**
5. **GND**
6. **Source 4**
7. **Drain 4**
8. **Input 4**
9. **Input 3**
10. **Drain 3**
11. **Source 3**
12. **NC**
13. **V+ (Substrate)**
14. **Source 2**
15. **Drain 2**
16. **Input 2**

**.072”**

**.080”**

**6 5 4 3**

**11 12 13 14**

**7**

**8**

**9**

**10**

**2**

**1**

**16**

**15**

**B**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: B**

**APPROVED BY: DK DIE SIZE .072” X .080” DATE: 10/20/16**

**MFG: SILICONIX THICKNESS .016” P/N: DG201B**

**DG 10.1.2**

#### Rev B, 7/1